Amendments to the Specification:

Please insert prior to the paragraph at page 1, line 1, the following paragraph:

This application claims priority under 35 USC § 119(e)(1) of provisional application Serial No. (TBN), filed February 26, 2004.

Please replace the first paragraph of page 3 with the following amended paragraph:

Most switching regulators do not implement a low power mode that maintains a [supply of] regulated output voltage. Many switching regulators that include a low power mode do not automatically sense the output current in an effort to make a determination of whether the low power mode should be entered or exited from. Furthermore, many of these switching regulators require a low power mode input signal to initiate the low power mode. There, however, are a few switching regulators that sense the output current and provide a feature of automatic entrance and exit from a low power mode. Unfortunately, these switching regulators require an expensive precision resistor or a current transformer to sense current and are dependent on the capacitor value and input and output voltage.

Please replace the first paragraph of page 4 with the following amended paragraph:

To address the above-discussed deficiencies of switching regulators, the present invention teaches a switching regulator having a low power control circuit that

automatically senses when the low power mode should be initiated without the use of expensive external components nor an extensive amount of external components. The switching regulator in accordance with the present invention includes a driver coupled to receive a first high side control signal [reference voltage]. An input switching device includes a control node that connects to the driver and a drain node that receives an input voltage. A diode couples between the source node of the input switching device and ground. A first end of an inductor connects to the node formed between the source node of the input switching device and the diode. A first output switching device includes a drain node connected to the second end of the inductor and a control node connected to a second high side control signal [output] node. A second output switching device includes a drain node connected to the second end of the inductor and a control node connected to a low side control signal [output] node. An output load and an output capacitor connect[s] between [to] the source nodes of the first and second output switching devices. A low power control circuit couples across the inductor to monitors the current across the output load and automatically initiates the low power mode of the switching regulator independent of the value of the output voltage, the output capacitor, the inductor [load] and the input voltage.

Please replace the second paragraph of page 4 with the following amended paragraph:

The low power control circuit includes a low power switching device that includes a control node connected to the high side control signal [output] node and a drain node connected to the second end of the inductor. An amplifier connects to the source node of the low power switching device and the first output switching device. A first current mirror

couples to the amplifier to mirror [the difference between] the output current delivered to [through] the output load through the first output switching device [and the current supplied at the second end of the inductor]. A second current mirror couples to the first current mirror to pass the mirrored output load current to a summing node, which is coupled to [mirror the current difference through] a current source and a capacitor [connected in parallel across the current source]. A comparator compares the voltage generated across [by] the capacitor with a predetermined voltage source. A first and second AND gate couples to the comparator. A first and second counter couple to the first and second AND gates respectively. The output of the first counter supplies a low power mode entry signal that initiates the low power mode for the switching regulator. The second AND gate couples to receive this low power mode entry signal. The output of the second counter supplies a low power mode exit signal that indicates when the switching regulator should exit [is not in] low power mode. The first AND gate couples to receive this low power mode exit signal.

Please replace the second paragraph of page 5 with the following amended paragraph:

Advantages of this design include but are not limited to a switching regulator that automatically enters into a low power mode without the requirement of an external signal. The switching regulator in accordance with the present invention does not require an expensive precision resistor coupled to the output to sense output current; nor does it require an additional feedback pin from the resistor. This embodiment does implement the use of an additional capacitor; yet, this capacitor can be a standard ceramic type with no special requirements. In addition, the capacitor's value can vary

widely without altering the performance of the switching regulator. This embodiment is also independent of input voltage, duty cycle, inductor value, output voltage, and most importantly output capacitance.

Please replace the first paragraph of page 8 with the following amended paragraph:

"side input switch T_1, whereas diode D_0 performs the function of the first low side input switch. In the alternative, D_0 could be substituted with a two other types of transistors, either MOS FET or BJT."

Please replace the second paragraph of page 8 with the following amended paragraph:

As shown, an input voltage V_{in1} is supplied to the drain node of input switching device T_1. The circuit driver D_1 connects to receive a high side input HSL_1. The output of circuit driver D_1 connects to the control node of input switching device T_1. The inductor L_1 couples between the source of the input switching device T_1 and the drain of the second output switching device T_2, while the source of second output switching device T_2 couples to ground. The drain of the first output switching device T_3 couples to inductor L_1. A high side control signal [output] HSL_2 coupled to the control node of the first output switching device T_3, while a low side control signal [output] LSL_1 couples to the control node of the second output switching device T_2. Capacitor C_{out1} and resistor R_{load1} couple in parallel across the source node of first output switching device T_3 and ground.

Please replace the third paragraph of page 8 with the following amended paragraph:

In operation, during buck mode, the input switching device T_1 is switched ON and OFF, while second output switching device T_2 is off completely and first output switching device T_3 is always on. When the input switching device T_1 turns off, node A_1 decreases to a voltage corresponding to diode D_0 below ground (-0.7V). The current [builds] decays in inductor L_1 because the voltage at node A_1 is lower [current for the driver D_1 is higher] than the output voltage, V_{out}. In the alternative, when the input switching device T_1 turns on, node A_1 increases in voltage. The current builds in inductor L_1 because the voltage at node A_1 is higher than the output voltage, V_{out}.

Please replace the first paragraph of page 9 with the following amended paragraph:

amplifier 10, a first current mirror 30, a second current mirror 32, a current source I_1, a capacitor C_1, a comparator 20, a first AND gate 22, a second AND gate 24, a first counter 26, [and] a second counter 28, and a set/reset latch 34.

Please replace the second paragraph of page 9 with the following amended paragraph:

Switching regulator 100 uses an external capacitor C_{out2} and the internal sense FETs, T_6 and T_7, to determine the load current under any condition. Once the load current is sensed, the control circuit 50 within switching regulator 100 generates to signal that initiates entry into the low power mode LP_{enter} or exit therefrom LP_{exit}. In addition, the

switching device T_7 in the present invention is a sense FET. Conventional switching regulators do not use a sense FET as a second high side switching device as switching device T_7 has been implemented in this design. Most conventional switching regulators are designed to implement the use of an external sense resistor or a current sense transformer.

Please replace the third paragraph of page 9 with the following amended paragraph:

As shown, an input voltage V_{in2} is supplied to the drain node of input switching device T_4. The circuit driver D_2 connects to receive a high side input HSL_3. The output of circuit driver D_2 connects to the control node of input switching device T_4. The inductor L_2 couples between the source of the input switching device T_4 and the drain of the second output switching device T_5, while the source of second output switching device T_5 couples to ground. The drain of the first output switching device T_6 couples to inductor L_2. A high side control signal [output] HSL_4 coupled to the control node of the first output switching device T_6, while a low side control signal [output] LSL_2 couples to the control node of the second output switching device T_5. Capacitor C_{out2} and resistor R_{load2} couple in parallel across the source node of first output switching device T_6 and ground.

Please replace the fourth paragraph of page 9 which continues on the first paragraph of page 10 with the following amended paragraph:

Low power control circuit 50 includes sense switching device T_7 which connects to amplifier 10. Specifically, the drain node of sense switching device T_7 connects to the second end of inductor L_2, the control node couples to the high side control signal [output] HSL_4, the source node couples to amplifier 10. Sense FET T_7 senses current in both the normal operating mode and the low power mode. Those skilled in the art may recognize that sense FET T_7 may be replaced with a similar switching device; yet, switching device T_7 must match switching device T_6 for the circuit to operate correctly. Once the load current is sensed[, given the value of capacitor C_1 is known,] the average output current can be derived, even without continuous current through the FET T_6.

Please replace the second paragraph of page 10 with the following amended paragraph:

Current mirror 30 couples between amplifier 10 and second current mirror 32. Current mirror 32 connects to current source I_1. Capacitor C_1 couples across current source I_1. Sensing FET T_7 [T_6]senses the current and [when the switching regulator goes into low power mode. Sense FET T_7 integrates] mirrors the current with that supplied to the load [processed] through [sense] FET T_6. This current is mirrored by current mirrors, 30 and 32, [The resultant signal is amplified and mirrored] into capacitor C_1. [Current i_2 pulls a constant current out of capacitor C_1, while sense FET T_6 adds current i_1 into the capacitor C_1.] This current is proportional to the output. It is subtracted from the reference current I_1. The difference is integrated by capacitor C_1. A voltage dependent on the output load appears at comparator 20. This voltage

enables the decision for entering and exiting the low power mode.

Please replace the third paragraph of page 10 with the following amended paragraph:

Comparator 20 couples to receive a voltage that is twice the value of the reference voltage V_{ref} and the voltage at node C_{LP}. Effectively, comparator C_1 compares the voltage generated by the capacitor with this predetermined voltage. A first and second AND gate, 22 and 24, couples to comparator C_1. A first and second counter, 26 and 28, couple to the first and second AND gates, 22 and 24, respectively. The output of the first counter 26 supplies a low power mode entry signal LP_{enter} that initiates the low power mode for the switching regulator 100. The set input of the set/reset latch 34 couples to receive this low power mode entry signal LP_{enter}. The second AND gate 24 couples to receive the output of the set/reset latch 34 [this low power mode entry signal LP_{enter}]. The output of the second counter 28 supplies a low power mode exit signal LP_{exit} that indicates when the switching regulator 100 [is not in] should exit low power mode. The reset input of the set/reset latch 34 couples to receive this low power mode entry signal LP_{exit}. The first AND gate 22 couples to receive the inverted output of the set/reset latch 34 [this low power mode exit signal LP_{exit}].

Please replace the fourth paragraph of page 10 with the following amended paragraph:

Specifically, comparator 20 compares the voltage across capacitor C_1 [current source I_1] with the value of two times the reference voltage V_{ref}. As shown, current i_1 is the

current that enters node C_{LP} and current i_2 is the current provided by current source I_1. When the average current i_1 becomes less than current i_2, comparator 20 will generate a signal LP_{enter} that signifies that switching regulator 100 may enter low power mode, wherein signal LP_{enter} will be "high". Counter 26 is a five bit counter that determines that switching regulator 100 will enter into low power mode after the signal is available over 32 cycles. Note that the value of counter 26 is not critical and may vary from one implementation to another. It is used to digitally filter the signal.

Please replace the first paragraph of page 11 with the following amended paragraph:

"OFF, while second output switching device T_5 is off completely and first output switching device T_6 is always on. When the input switching device T_4 turns off, node A_2 decreases to a voltage corresponding to diode D_0 below ground (-0.7V). The current [builds] decays in inductor L_2 because the voltage at node A_2 is lower [current for the driver D_2 is higher] than the output voltage, V_{out}. In the alternative, when the input switching device T_4 turns on, node A_2 increases in voltage. The current builds in inductor L_2 because the voltage at node A_2 is higher than the output voltage, V_{out}."

Please replace the third paragraph of page 11 with the following amended paragraph:

When switching device T_4 is high, switching device T_6 is on. Thereby, current flows through the inductor L_1 which produces a triangle wave. At the same time, switching device T_7 is on and senses the load current. Amplifier 10 creates a ratio metric current from switching device T_6 in switching device T_7 [mirrors the difference between the current sensed by sense switching device, T_7 and T_6], using current mirror 30 implemented by transistors, 12 and 14. The current through current mirror 30 is further mirrored by current mirror 32 implemented by 16 and 18 to provide current i_1 which is proportional to the load current. The sense FET T_7 and amplifier 10 provide a current that is proportional to the current through switching device T_6.

Please replace the fourth paragraph of page 11 with the following amended paragraph:

During the determination of whether the switching regulator 100 should enter the [enter] low power mode, it is assumed that the voltage on the C_{LP} pin is above twice the reference voltage V_{ref}, since it is pulled high during the startup of the device. [In any of the operating modes, the average output amplifier and the external capacitor.] If the average (sense FET mirrored) current i_1 is less than the current of the trimmed current source I_1, the voltage at node C_{LP} will start to decrease. Once the voltage drops below twice the reference voltage V_{ref}, the comparator signals the LPModeSignal which goes into a 5-bit up counter. If 32 consecutive LPMode signals are received, then the part enters low power mode. This works for all modes, buck, boost, and buck-boost, since the average output current is always

delivered through the T_4 FET. An example of entering low power mode is shown in Fig. 4.

Please replace the first paragraph of page 12 with the following amended paragraph:

the output load R_{load2} and the output capacitance C_{out2}, with a hysteric operation determined by the comparators of the output voltage. When this is occurring, the current through switching device T_6 is discontinuous, with the output current supplied by the charge on the large output capacitor C_{out2}. In the same manner described previously for the normal mode of operation, to [To] sense output current during this case, a ratio of the output charge placed on the output capacitor C_{out2} is placed on capacitor C_1 and slowly bled off by a fixed internal current source I_1. If the charge placed on capacitor C_1 is less than the fixed internal sources time/current relationship, then the output current is less than the threshold, and switching regulator 100 stays in low power mode. If the charge increases above the internal current source threshold for two consecutive cycles, switching regulator 100 exits low power mode and runs at the standard fixed switching frequency.

Please replace the third paragraph of page 12 with the following amended paragraph:

In boost mode and buck-boost mode, the switching regulator will function similar to that of buck mode with the following exceptions. Specifically, in boost mode, the first output switching device T_6 and the second output switching device T_5 are switched ON and OFF out of phase with each other. In buck-boost mode, the input switching device T_4 and

the second output switching device T_5 are switched ON and OFF in phase with each other, and the first output switching device T_6 is switched ON and OFF out of phase with the input switching device T_4 and second output switching device T_5.

Please replace the second paragraph of page 14 with the following amended paragraph:

Advantages of this design include but are not limited to a switching regulator having a control circuit that automatically determines when the switching regulator will enter or exit a low power mode without the requirement for an external signal. It does not require an expensive precision resistor on the output to sense output current, as well as an additional feedback pin from the resistor. It does require an additional capacitor, however, this capacitor can be a standard ceramic type with no special requirements. It's value can vary widely and the system will still work correctly. It is also independent of input voltage, duty cycle, <u>inductance, output voltage</u>, and most importantly output capacitance.

Please replace the third paragraph of page 14 with the following amended paragraph:

Since entrance and exit from the low power mode occurs automatically with a separate external capacitor C_1 that is independent from the output capacitor C_{out2} <u>as well as</u> [nor] the input voltage, this circuit will work with any value of an output capacitor or any input voltage without affecting the point where the switching regulator exits or enters the low power mode. Most known switching regulators point of entry or exit into and out of the low power mode, however, are effected